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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	table near layout near elastic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/02/01 16:38
L2	98	table near layout and cell and size and height and width and row and column	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/02/01 16:40
L3	1326	(715/500).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 16:50
L4	67714	display and space and requirement and reduce and element	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/02/01 16:51
L5	1631	display same space same requirement and reduce and element	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/02/01 16:51
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L7	81	display same space same requirement same reduce same element	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/02/01 16:56
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Constraint Cascading Style Sheets for the Web (1999) (Make Corrections) (16 citations)

Greg J. Badros, Alan Borning, et al.

ACM Symposium on User Interface Software and Technology

Abstract: Cascading Style Sheets have recently been introduced by the W3C as a mechanism for controlling the appearance of HTML documents. In this paper, we demonstrate how constraints provide a powerful unifying formalism for declaratively understanding and specifying style sheets for web documents. With constraints we can naturally and declaratively specify complex behaviour such as inheritance of properties and cascading of conflicting style rules. We give a detailed description of a constraint-based ... (Update)

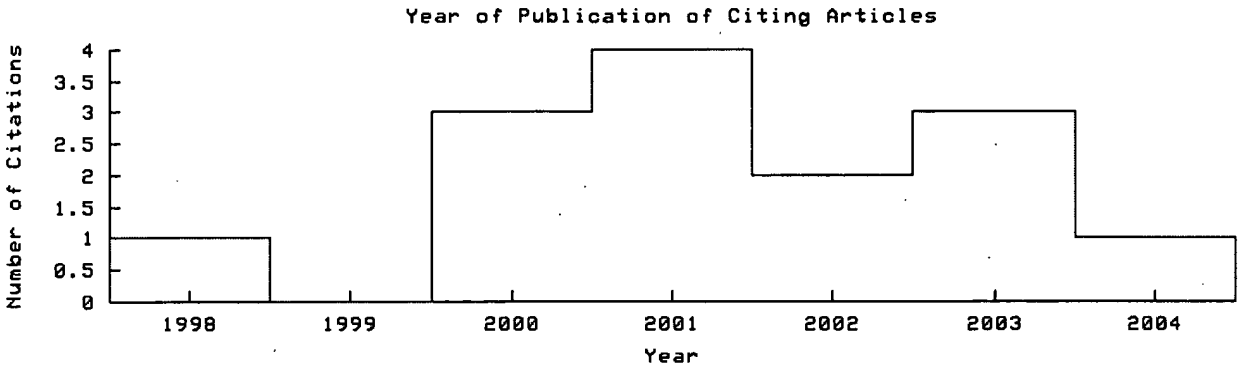
BibTeX entry: (Update)

G. J. Badros, A. Borning, K. Marriott, and P. Stuckey. Constraint cascading style sheets for the web. In Proceedings of the 1999 ACM Conference on User Interface Software and Technology, November 1999.
http://citeseer.ist.psu.edu/article/badros00constraint.html More

```
@inproceedings{ badros99constraint,
    author = "Greg J. Badros and Alan Borning and Kim Marriott and Peter J. Stuckey",
    title = "Constraint Cascading Style Sheets for the Web",
    booktitle = "{ACM} Symposium on User Interface Software and Technology",
    pages = "73-82",
    year = "1999",
    url = "citeseer.ist.psu.edu/article/badros00constraint.html" }
```

Citations (may not include all citations):
127 Sketchpad: A man-machine graphical communication system (context) - Sutherland - 1963
96 Lisp and Symbolic Computation (context) - Borning, Freeman-Benson et al. - 1992
87 Programming with Constraints: An Introduction (context) - Marriott, Stuckey - 1998
75 Garnet: Comprehensive support for graphical highly interacti.. (context) - Myers, Giuse et al. - 1990
61 The Amulet environment: New models for effective user interf.. - Myers, McDaniel et al. - 1997 DBLP
40 Solving linear arithmetic constraints for user interface app.. - Borning, Marriott et al. - 1997 ACM DBLP
39 The Cassowary linear arithmetic constraint solving algorithm.. - Badros, Borning - 1998
20 Cascading style sheets (context) - Bos, Lie et al. - 1998 ACM

11 Interactive physically-based manipulation of discrete/contin.. - Harada, Witkin et al. - 1995 ACM DBLP
10 Constraints for the web (context) - Borning, Lin et al. - 1997 ACM DBLP
10 PSL: An alternate approach to style sheet languages for the .. - Marden, Munson - 1998 DBLP
7 Technical report (context) - Consortium, specification - 1998
4 Frame-based layout via style sheets (context) - Bos, Raggett et al.
4 Positioning HTML elements with cascading style sheets (context) - Furman, Isaacs
4 Flexible font-size specification in Web documents - Lin, Marriott et al. - 1999
4 Amaya web browser software (context) - Consortium - 1998
1 A high-level language for specifying pictures (context) - Wyk - 1982



The graph only includes citing articles where the year of publication is known.

Documents on the same site (http://128.95.4.112/homes/gjb/): More
An Empirical Analysis of C Preprocessor Use - Ernst, Badros, Notkin (1997) (Correct)
A Framework for Preprocessor-Aware C Source Code Analyses - Badros (1998) (Correct)
Constraints in Interactive Graphical Applications - Badros (1998) (Correct)

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Nguyen, H.T.; Chattejee, A.;
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Volume 8, Issue 4, Aug. 2000 Page(s):419 - 424
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Cocchini, P.; Pedram, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 19, Issue 3, March 2000 Page(s):339 - 349
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3. **Empirical performance evaluation methodology and its application to page segmentation algorithms**
Song Mao; Kanungo, T.;
Pattern Analysis and Machine Intelligence, IEEE Transactions on
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AbstractPlus | References | Full Text: PDF(1316 KB) **IEEE JNL**
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4. **Understanding and reducing Web delays**
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Computer
Volume 34, Issue 12, Dec. 2001 Page(s):30 - 37
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5. **The Structure and Operation of a Relational Database System in a Cell-Oriented Integrated Circuit Design System**
Hollaar, L.; Nelson, B.; Carter, T.; Lorie, R.A.;
Design Automation, 1984. 21st Conference on
25-27 June 1984 Page(s):117 - 125
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Published before June 2001
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1 The table layout problem

Richard J. Anderson, Sumeet Sobti

June 1999 **Proceedings of the fifteenth annual symposium on Computational geometry SCG '99**

Publisher: ACM Press

Full text available: pdf(1.15 MB) Additional Information: full citation, references, citings, index terms

2 CLIP: integer-programming-based optimal layout synthesis of 2D CMOS cells

Avaneendra Gupta, John P. Hayes

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Publisher: ACM Press

Full text available: pdf(371.02 KB) Additional Information: full citation, abstract, references, index terms

A novel technique, CLIP, is presented for the automatic generation of optimal layouts of CMOS cells in the two-dimensional (2D) style. CLIP is based on integer-linear programming (ILP) and solves both the width and height minimization problems for 2D cells. Width minimization is formulated in a precise form that combines all factors influencing the 2D cell width—transistor placement, diffusion sharing, and vertical in ...

Keywords: CMOS networks, circuit clustering, diffusion sharing, integer linear programming, integer programming, layout optimization, leaf cell synthesis, module generation, transistor chains, two-dimensional layout

3 Modeling layout tools to derive forward estimates of area and delay at the RTL level

Donald S. Gelosh, Dorothy E. Steliff

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Publisher: ACM Press

Full text available: pdf(278.32 KB) Additional Information: full citation, abstract, references, index terms

Forward estimates of area and delay facilitate effective decision-making when searching the solution space of digital designs. Current estimation techniques focus on modeling the layout result and fail to deliver timely or accurate estimates. This paper presents a novel approach to deriving these area and delay estimates at the RTL level by modeling the layout tool, rather than the layout result. This approach uses machine learning techniques to capture the relationships between general des ...

Keywords: VLSI CAD, estimation, estimation techniques, layout, machine learning

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1 Cell-based hierarchical pitchmatching compaction using minimal LP

So-Zen Yao, Chung-Kung Cheng, Debaprosad Dutt, Surendra Nahar, Chi-Yuan Lo
July 1993 **Proceedings of the 30th international conference on Design automation DAC '93**
Publisher: ACM Press
Full text available: pdf(531.59 KB) Additional Information: full citation, references, index terms

2 Layout techniques supporting the use of dual supply voltages for cell-based designs

Chingwei Yeh, Yin-Shuin Kang, Shan-Jih Shieh, Jinn-Shyan Wang
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation DAC '99**
Publisher: ACM Press
Full text available: pdf(145.89 KB) Additional Information: full citation, references, citings, index terms

3 Strip layout: a new layout methodology for standard circuit modules

J. Apte, G. Kedem
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation DAC '87**
Publisher: ACM Press
Full text available: pdf(681.69 KB) Additional Information: full citation, abstract, references, index terms

In this paper we describe Strip Layout, a new layout methodology that is suitable for automatically laying out standard circuit modules and for automatic module generation from transistor net-list. We demonstrate that the new layout methodology yields circuits that are denser than standard cell layout while retaining all the advantages of standard cells. Moreover, Strip Layout could be generated by simple algorithms at high speed.

4 A new hierarchical layout compactor using simplified graph models

W. Kim, J. Lee, H. Shin
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation DAC '92**
Publisher: IEEE Computer Society Press
Full text available: pdf(398.30 KB) Additional Information: full citation, references, citings, index terms

5 Width minimization of two-dimensional CMOS cells using integer programming

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SRAM **cell**", Electron Devices Meeting, 2002. IEDM. 2002. Digest. International, pp. 61 -64, December 2002. [2] Mike Reinhardt, "**Automatic Layout** Migration", ...